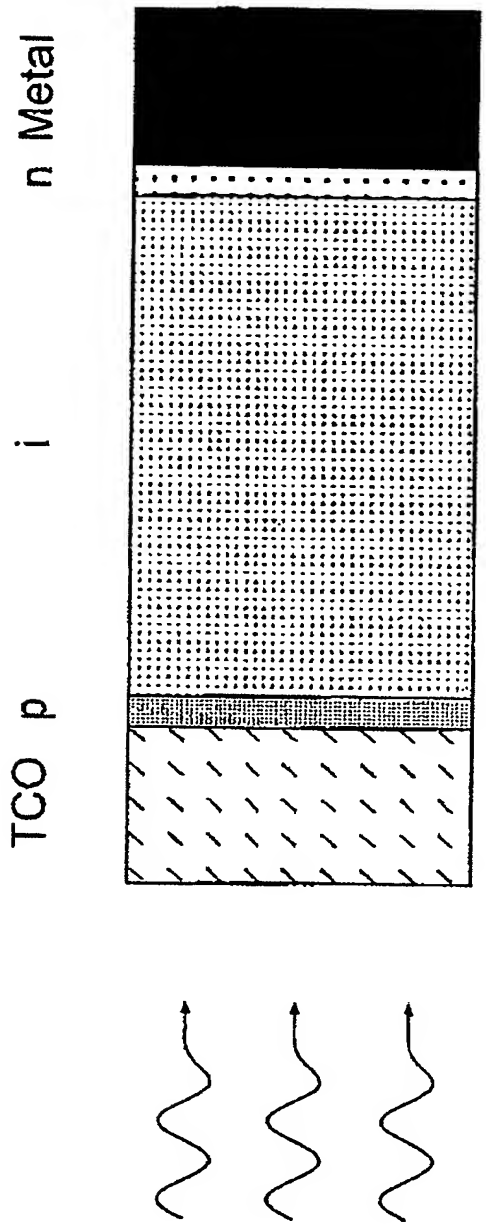

Fig. 1

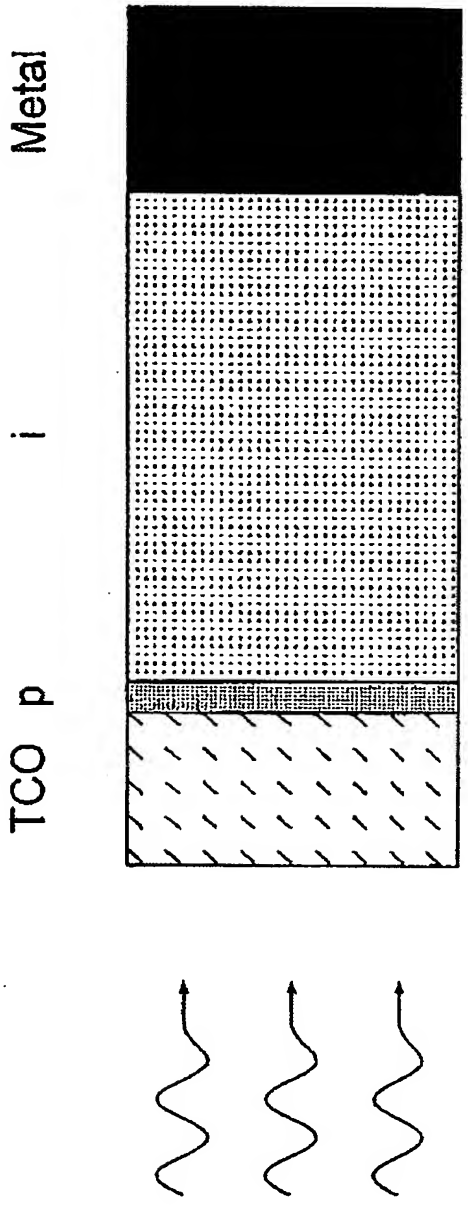

Fig. 2

Fig. 3

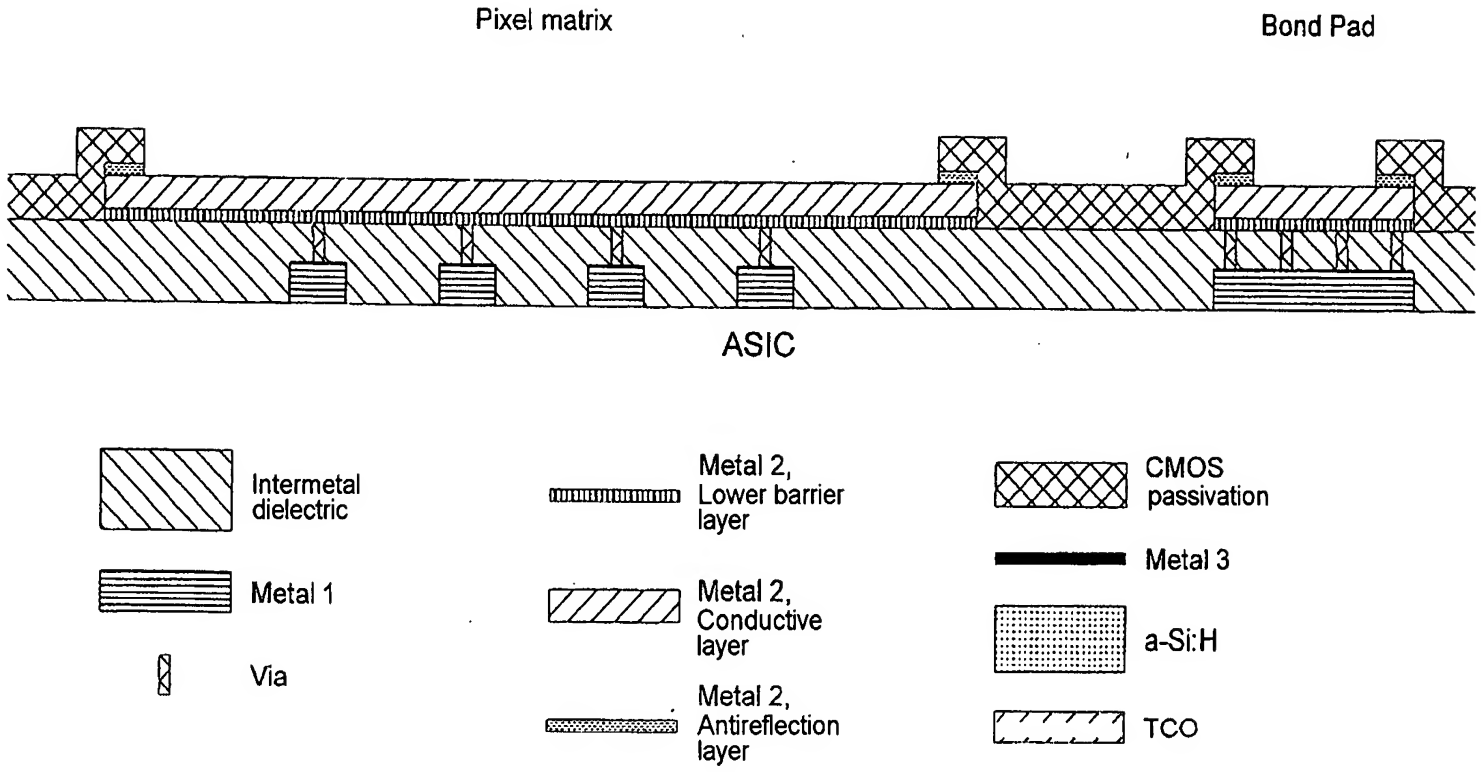

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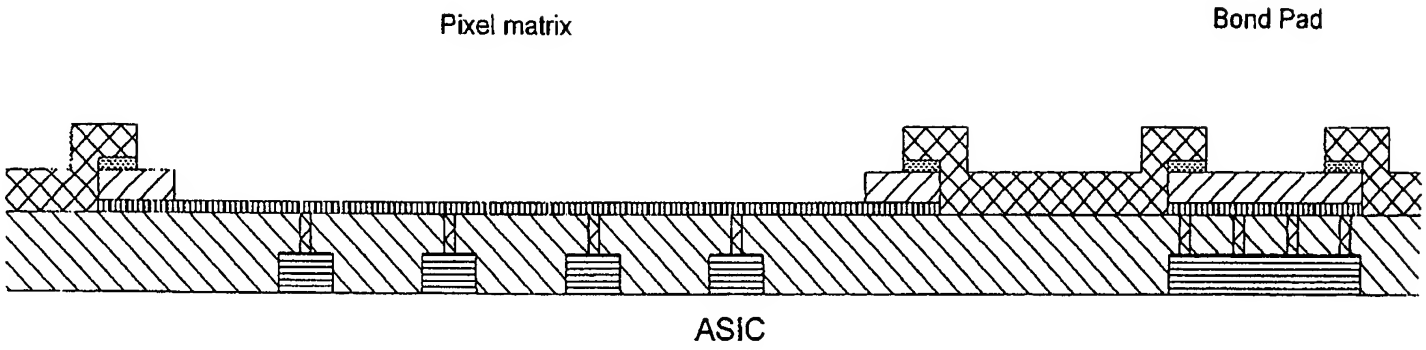
Fig. 4


Pixel matrix
Bond Pad
ASIC
Intermetal dielectric
Metal 1
Via
Metal 2, Lower barrier layer
Metal 2, Conductive layer
Metal 2, Antireflection layer
CMOS passivation
Metal 3
a-Si:H
TCO

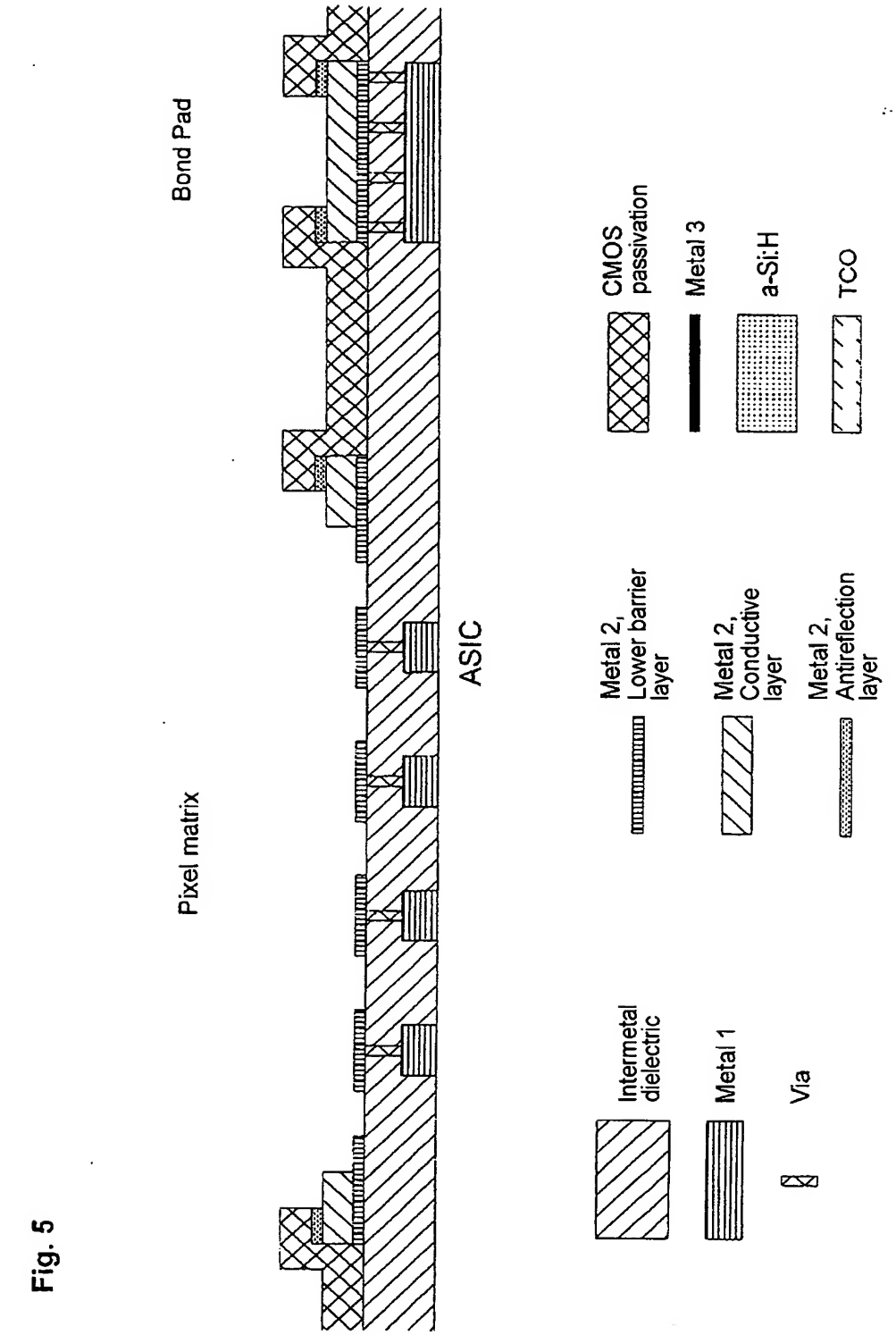

Bond Pad
Pixel matrix
ASIC
CMOS passivation
Metal 3
a-Si:H
TCO
Metal 2, Lower barrier layer
Metal 2, Conductive layer
Metal 2, Antireflection layer
Intermetal dielectric
Metal 1
Via

Fig. 5

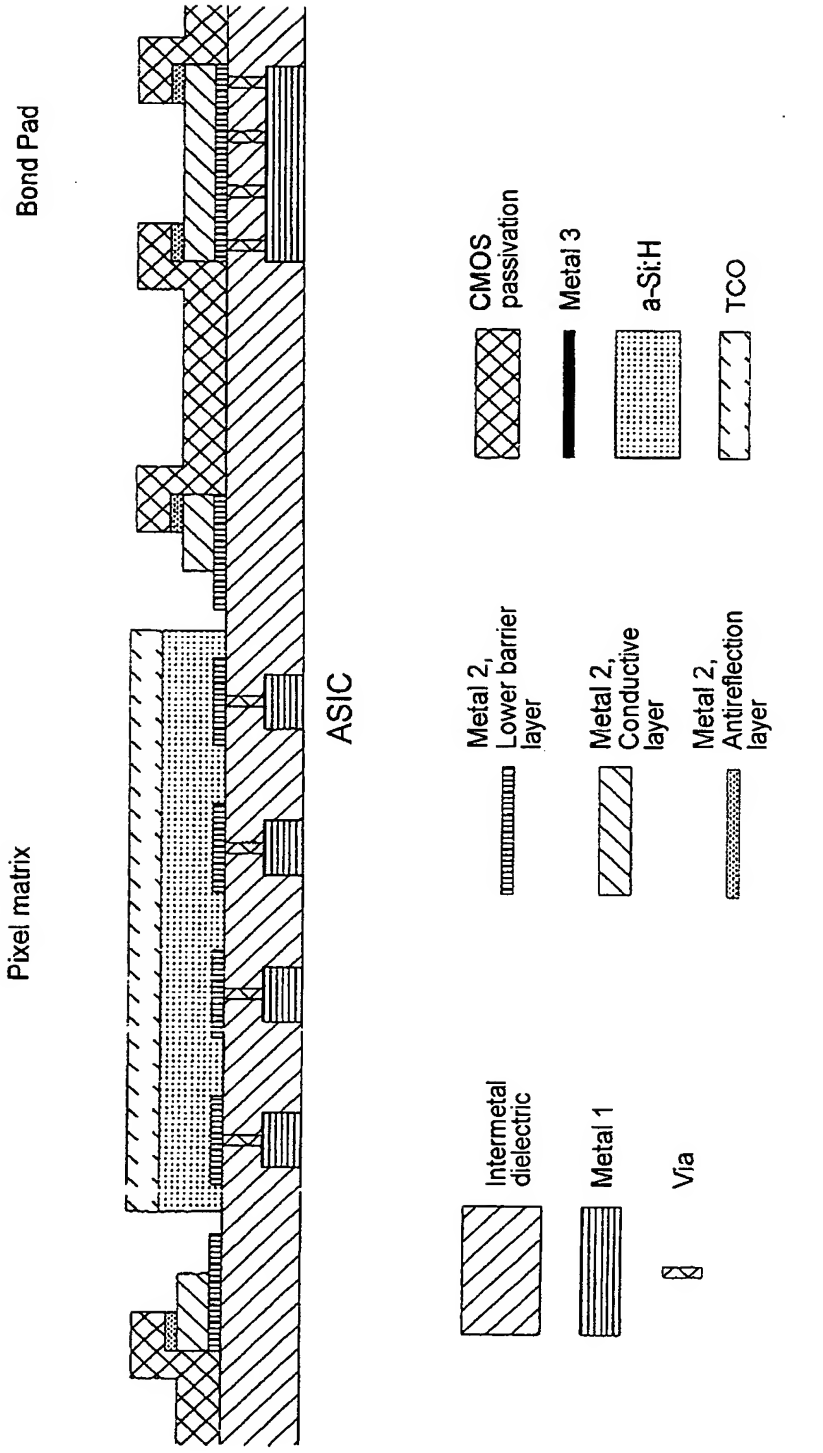

Bond Pad
Pixel matrix
ASIC
CMOS passivation
Metal 3
a-Si:H
TCO
Metal 2, Lower barrier layer
Metal 2, Conductive layer
Metal 2, Antireflection layer
Intermetal dielectric
Metal 1
Via

Fig. 6

Fig. 7

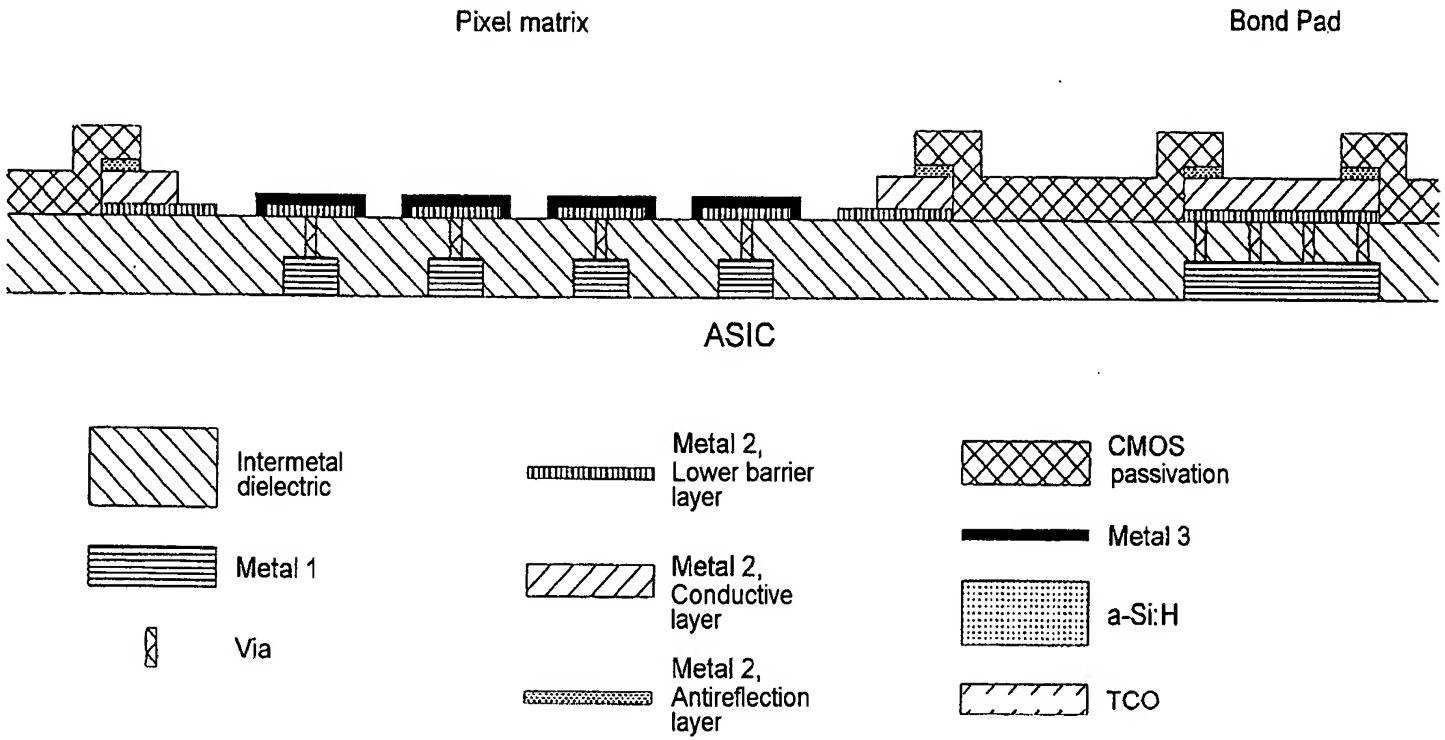


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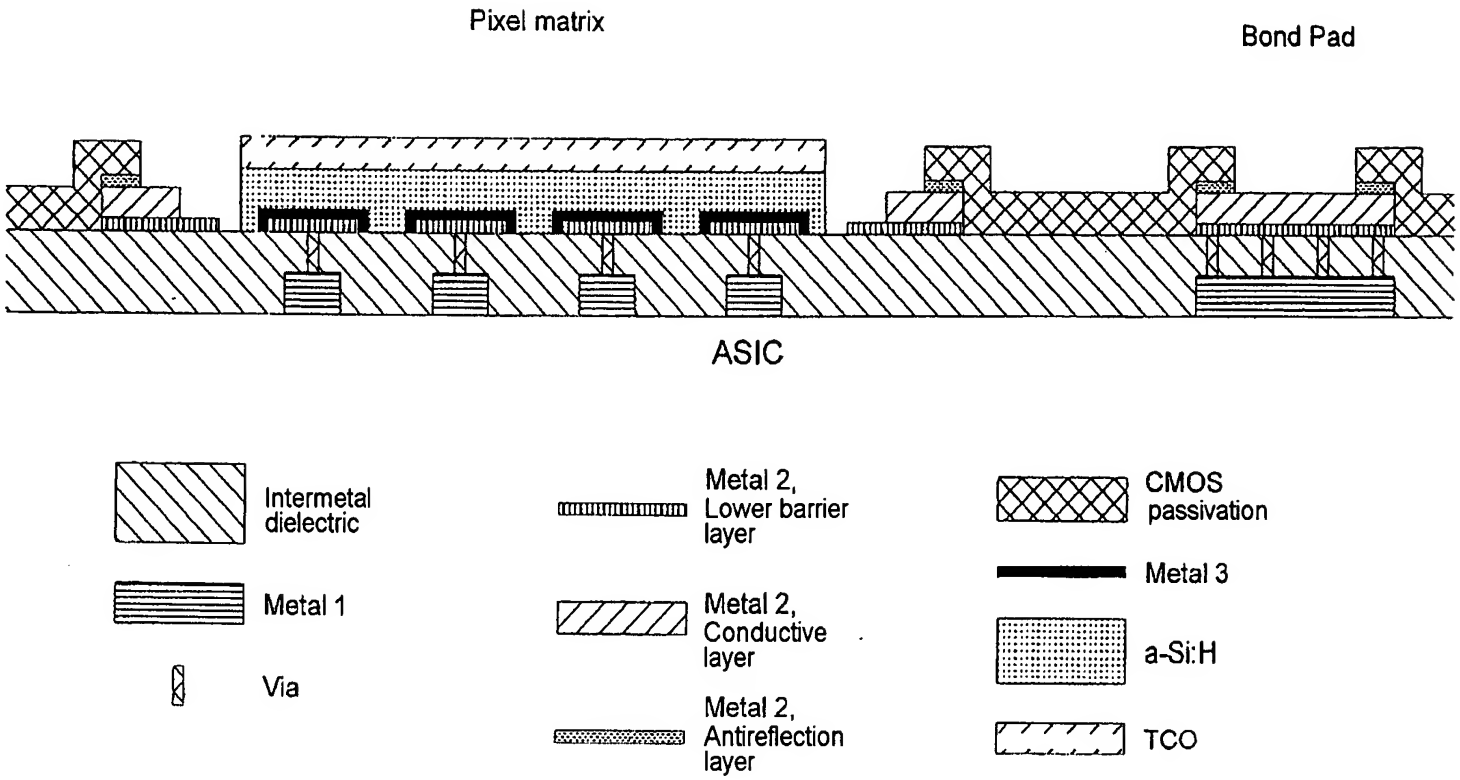
Fig. 8


Pixel matrix
Bond Pad
ASIC
Intermetal dielectric
Metal 1
Via
Metal 2, Lower barrier layer
Metal 2, Conductive layer
Metal 2, Antireflection layer
CMOS passivation
Metal 3
a-Si:H
TCO

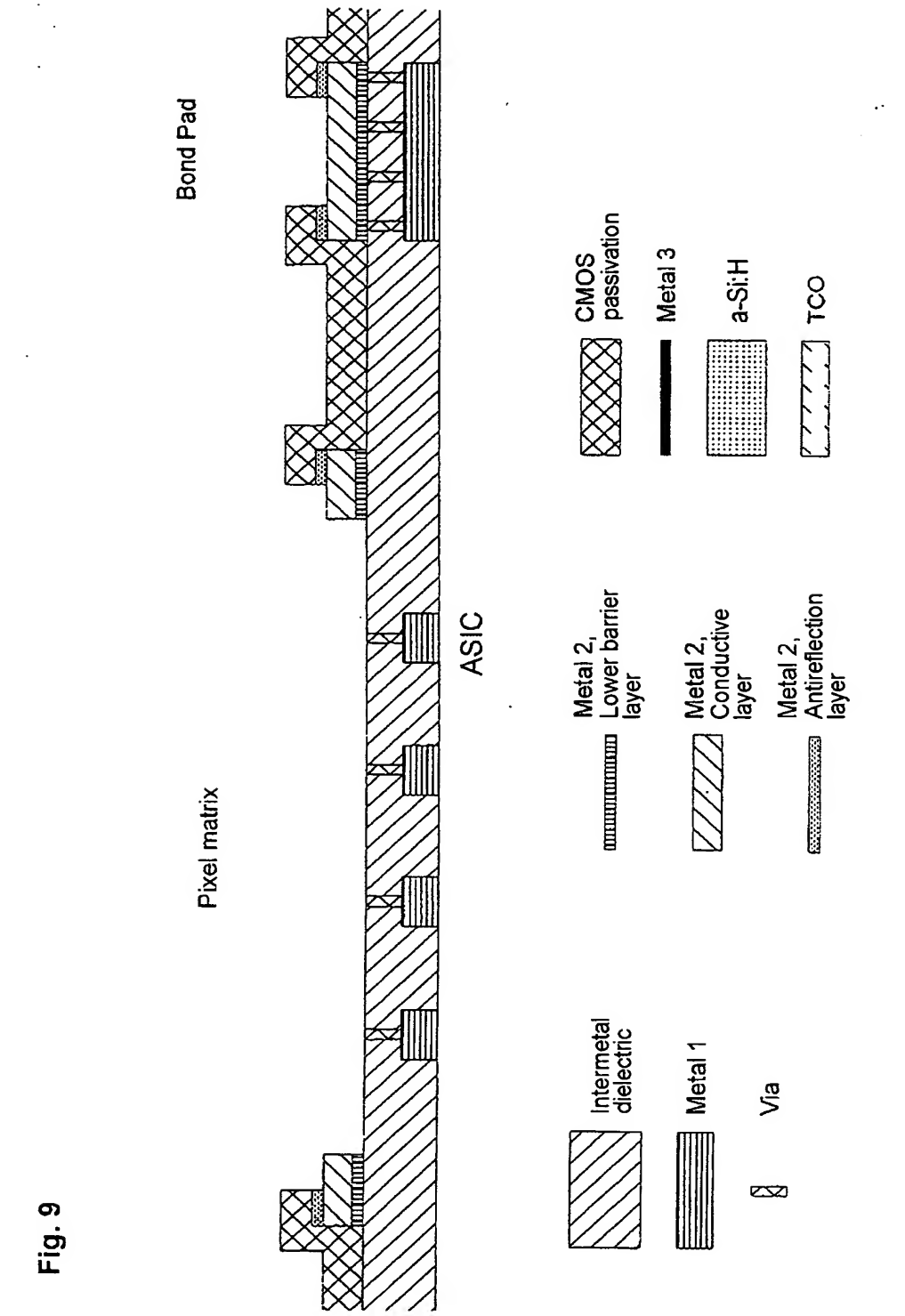

Bond Pad
Pixel matrix
ASIC
CMOS passivation
Metal 3
a-Si:H
TCO
Metal 2, Lower barrier layer
Metal 2, Conductive layer
Metal 2, Antireflection layer
Intermetal dielectric
Metal 1
Via

Fig. 9

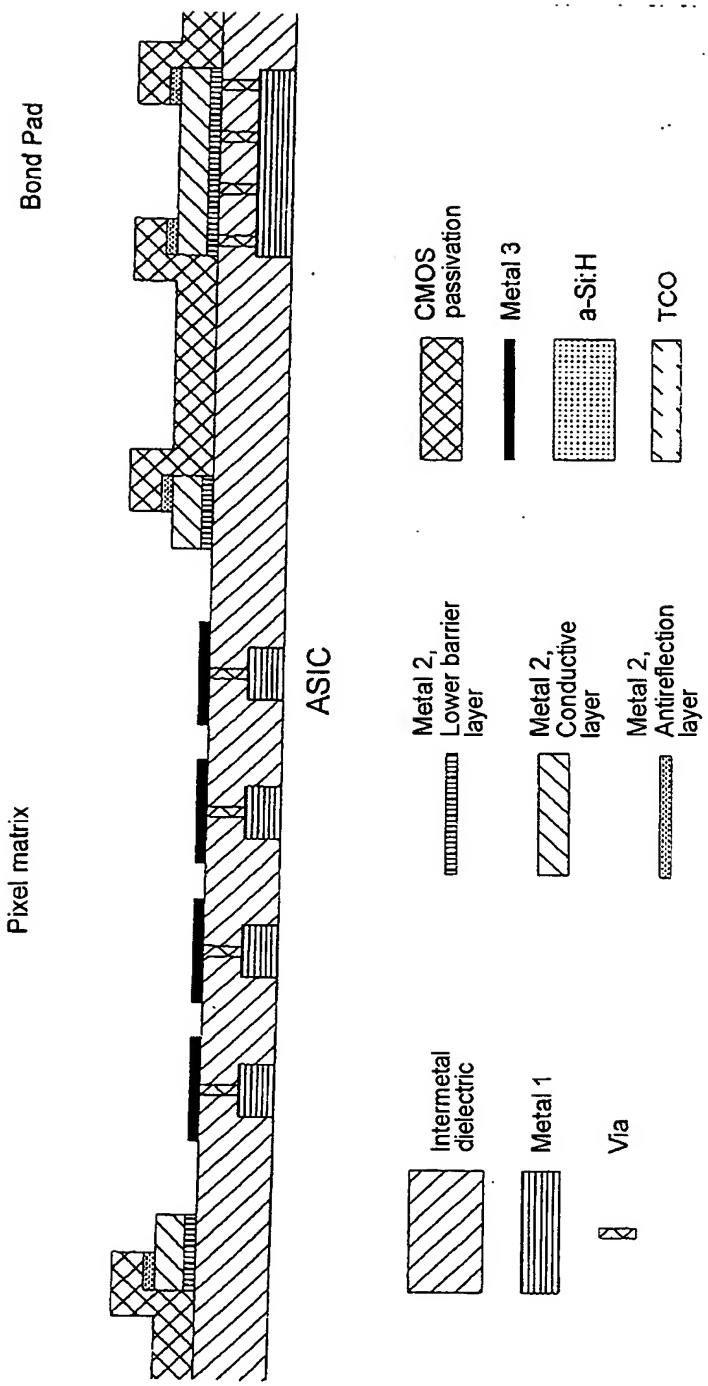

Bond Pad
Pixel matrix
ASIC
CMOS passivation
Metal 3
a-Si:H
TCO
Metal 2, Lower barrier layer
Metal 2, Conductive layer
Metal 2, Antireflection layer
Intermetal dielectric
Metal 1
Via

Fig. 10

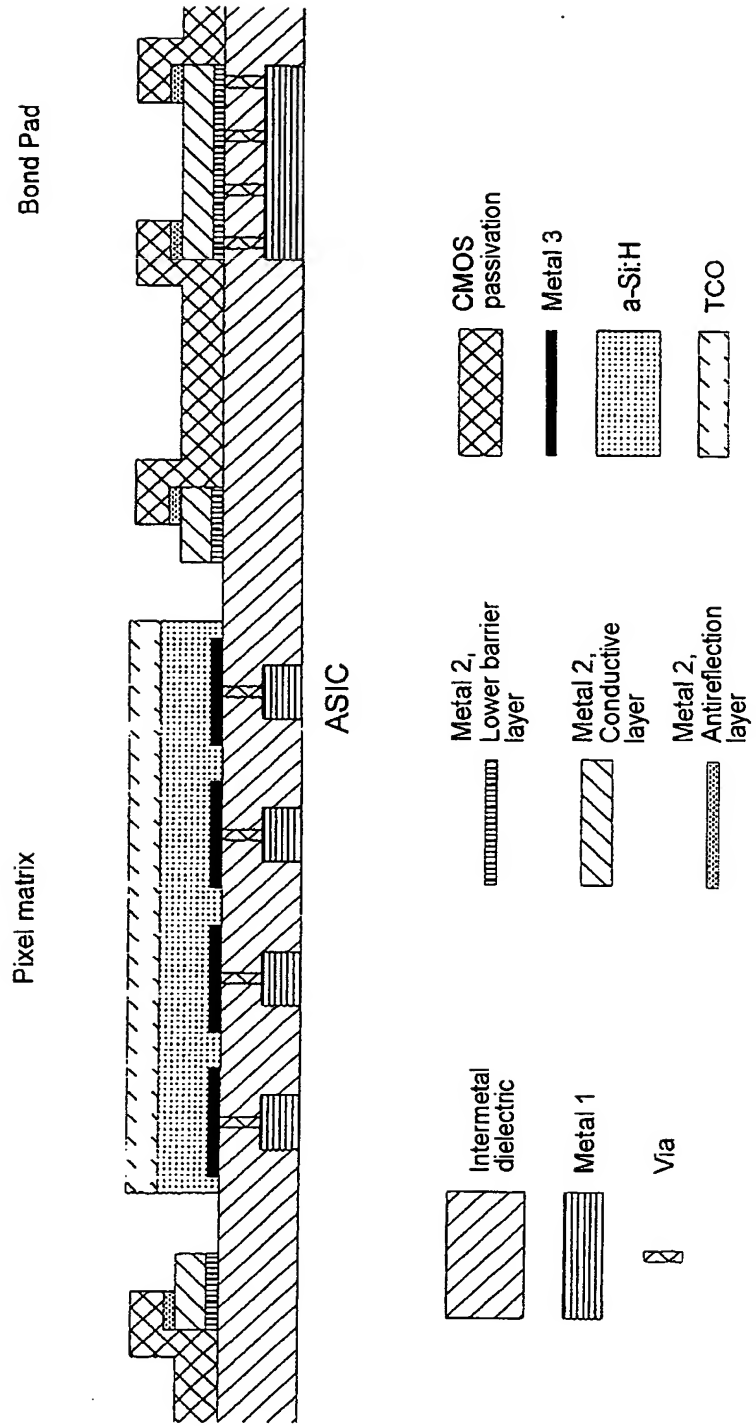

Bond Pad
Pixel matrix
ASIC
CMOS passivation
Metal 3
a-Si:H
TCO
Metal 2, Lower barrier layer
Metal 2, Conductive layer
Metal 2, Antireflection layer
Intermetal dielectric
Metal 1
Via

Fig. 11